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(54) Superconducting electronic structures and methods of preparing same.

(57) A superconducting electronic circuit device, useful when impedance matching is desired, especially suited to microwave frequencies, consisting of a thin dielectric layer (12) with superconducting layers (10,14) on both sides. A superconductor such as Yttrium Barium Copper Oxide (YBCO) is formed on a first substrate (12) such as lanthanum aluminate. A protective layer (16) like gold is deposited on the YBCO and a second carrier substrate (20) is bonded to the protected YBCO. The first substrate (12) is then thinned into a thin dielectric film and a second layer (14) of superconductor is epitaxially grown thereon to create the desired circuits.

FIG. 2

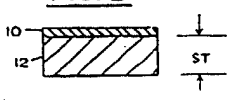


FIG. 3

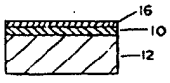


FIG. 4

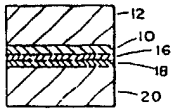


FIG. 5

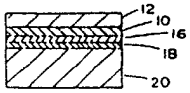
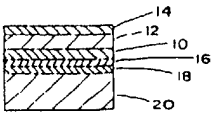


FIG. 6



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This invention concerns the production of so-called superconducting electronic structures such as electronic circuit devices that handle signals over a broad range of frequencies, particularly the higher, more demanding, microwave frequencies. We will describe, more specifically, devices made from superconducting materials, especially high critical temperature (Tc) superconductors (HTS).

Background of the Invention

Electronic devices that operate from low frequencies up through the microwave portion of the spectrum are important for communication, data processing, and other applications. These devices include transmission lines, filters, resonators, delay lines and other structures. The performance of these devices can be enhanced by the use of superconducting materials, which offer lower resistive losses and lower dispersion of signals than normal metal conductors such as copper or gold.

Conventional superconductors, such as elemental niobium, require devices to be operated at temperatures near the boiling point of liquid helium (4 degrees Kelvin), a difficult and costly temperature to maintain. Higher Tc superconductors permit devices to operate at or near the more practical boiling point of liquid nitrogen (77 degrees Kelvin). The newer high Tc superconductors are members of a class of layered perovskite compounds in which electronic transport takes place in planes formed by copper and oxygen atoms. As a result, these materials are referred to as copper oxide superconductors or simply cuprates. Examples include varying stoichiometric compounds of YBaCuO, LaSrCuO, BisrCaCuo, and TlBaCaCuO. Of particular interest is the compound composed of yttrium, barium, copper, and oxygen (YBCO) in the ratios of 1:2:3:7.

The application of HTS technology to electronic devices, especially in the microwave region of the electromagnetic spectrum, has been complicated by the fabrication requirements for HTS films. In particular, the basic device geometry needed for microwave components is difficult to achieve with the materials and methods currently in practice. Typical microwave circuit elements and general impedance matched transmission lines consist of a ground plane metallization, a dielectric layer overlaying the ground plane, and a thin strip conductor layer, on top of the dielectric layer, that contains the active circuit. Alternating current signal propagation is primarily by electromagnetic waves traveling in the dielectric layer between the ground plane and the thin strip.

The circuit elements need to be impedance matched for efficient and reflection free operation. The impedance of the structure is determined by the thickness of the dielectric layer, its dielectric constant, and the width of the conducting strip. For standard 50 ohm impedances, commonly used dielectric materials dictate dielectric thicknesses comparable to the line widths of the conducting layer. In densely packed circuits, with line widths on the order of a few microns, dielectric thickness must also be on the order of only a few microns.

The difficulty of fabricating high temperature superconducting films on opposite sides of a very thin dielectric layer, perhaps as thin as a few microns, has restricted the development of HTS microwave devices. Common sense suggests two possible approaches to this problem. The first approach would be to deposit superconductor film on opposite sides of a thin dielectric substrate such as lanthanum aluminate or sapphire. The second approach would be to deposit the layers sequentially (superconductor, dielectric, superconductor) on a thick substrate. Unfortunately, neither of these approaches is practical because of the essential requirements for depositing thin HTS films.

The advantageous properties of HTS films are available only in samples grown with a high degree of crystalline order. To maintain this order, high quality HTS films are preferably grown on substrate materials that do not interact chemically with the film and that have crystal structures which permit oriented growth of the superconductor. Substrates that are lattice-matched to the superconductor, such as lanthanum aluminate or strontium titanate, are particularly well suited to this purpose as they provide a nearly ideal template for epitaxial growth of the superconductor thereon.

Some otherwise desirable substrates, such as sapphire and silicon, fail to satisfy one or more of the criteria stated above, lacking chemical stability with HTS films or a close lattice match. Nevertheless, it is still possible to grow high quality HTS films on silicon and sapphire by depositing a thin buffer layer between the substrate and the HTS film.

HTS films are generally formed by vaporizing the constituent components of the HTS material and allowing them to impinge upon a substrate. The components may be vaporized by laser ablation, sputtering, or other techniques. The substrate must be maintained at a temperature suitable for forming the proper crystal structure, typically above 700 degrees C., in an oxygen rich environment. In order to grow HTS films with uniformly excellent properties on substrates of technologically useful sizes (1 to 5 square centimeters), it is necessary to control the temperature of the substrate within a narrow range over the entire area of the substrate. To achieve this temperature control, the substrate is clamped or tightly bonded to a heater. It is also possible to control the temperature by radiation

heating.

These heating techniques necessarily subject the thin brittle substrates to mechanical and thermal stresses, leading to an unacceptable amount of breakage even in substrates as thick as 250 microns. Clearly, substrates that are ten or even a hundred times thinner would have no structural integrity without continuous physical support. Thus, it is very difficult to deposit HTS films on opposite sides of such a thin dielectric substrate, in accordance with the first common sense approach mentioned above and the challenge is further exacerbated as the substrate thickness is reduced. And yet, substrates with thicknesses of 250 microns or greater place unacceptable constraints on line widths and component densities in microwave circuits.

The second common sense approach is to sequentially deposit layers of superconductor, dielectric, and superconductor on an appropriate substrate. Whereas the strategy of the first approach is unworkable because free standing substrates under 250 microns are too thin to work with, the strategy of the second approach fails because it is not practical to deposit thick dielectrics. It is very hard to grow dielectric materials with the desired crystalline quality and dielectric properties in thicknesses over a half micron. If the crystalline structure is poor, it will not support the growth of the second layer of superconductor. If the quality of the dielectric or superconductor is poor, the device performance will be degraded.

We will describe arrangements which allow the construction of useful devices from high Tc superconductors spaced by a suitably thin dielectric substrate.

We will describe the fabrication of practical and robust HTS devices with dielectric layer thicknesses in the range of 1 to 250 microns. A novel fabrication sequence is described that begins with the deposition of an HTS film on a first substrate thick enough to be conveniently handled. The superconductor is then covered with a special protective layer that controls the migration of oxygen out of and into the superconductor. The protective layer also prevents the reaction of the superconductor with future layers during processing and film growth. Copper-oxide superconductors are very reactive, and any disruption of their stoichiometry or crystal structure quickly degrades their superconductivity.

The protected superconductor layer is then bonded to a second carrier substrate so that the superconductor is mechanically sandwiched between two stabilizing substrates. So stabilized, the original first substrate can now be machined and polished as thin as desired to form a dielectric layer from 1 to 250 microns thick as needed. The second superconductor is then deposited onto the dielectric layer to complete the superconductor-dielectric-superconductor (SDS) structure. This SDS structure is appropriate and useful not only for microwave circuits, but also for components, devices, and circuits operating at any frequency, even in direct current applications where impedance matching is desirable.

Additional details and benefits are described hereinafter with reference to the drawings which show various preferred embodiments of the invention.

Brief Description of the Drawings

Figure 1 is a perspective view of a fragmentary portion of the operative layers of the desired SDS structure resulting from the fabrication sequence of the present invention.

Figures 2-6 show the sequential steps used to produce the structure of Figure 1 as follows:

Figure 2 shows the deposited first superconductor layer on a first substrate;

Figure 3 shows the addition of a protective layer on the first superconductor layer;

Figure 4 shows the Figure 3 structure bonded to a carrier substrate to mechanically stabilize the structure;

Figure 5 shows the first substrate reduced in thickness to create a thin dielectric layer; and

Figure 6 shows the addition of the second superconductor to create the SDS structure.

Figure 7 shows another embodiment of the invention similar to Figure 2 except with a buffer layer interposed between the first substrate and the first superconductor layer.

Figure 8 shows the SDS structure of Figure 6 with buffer layers interposed between the dielectric layer and both superconducting layers.

Figure 1 depicts a typical portion of a superconducting microwave circuit using the SDS structure. The essential elements are a ground plane superconductor layer 10, a thin dielectric layer 12, and a strip of superconducting material 14. Signals propagate primarily in the form of electromagnetic waves in the dielectric layer 12 bounded by the ground plane 10 and the strip 14. Strip 14 can be made very long to create devices such as a signal delay line, or formed with capacitively coupled gaps to create filters or resonators, or simply used as a signal carrying transmission line. For the typically used characteristic impedance, the dielectric thickness DT needs to be on the order of the line width LW. To achieve the required circuit packing density compatible with contemporary designs, LW may be as small as one micron, which means that DT may have to be as thin as one micron. Figures 2-6 illustrate the stages of a method of creating the

unique SDS structure of Figure 1 using HTS films and compatible dielectrics that allows DT to be in the range of 1 to 250 microns.

In Figure 2, a first layer of superconducting material 10 has been epitaxially grown on a first substrate 12. YBCO is the preferred superconductor, while lanthanum aluminate or magnesium oxide are the preferred substrate materials. The particular method of growing or depositing the superconducting films is not critical to this invention. The preferred deposition processes are laser ablation and off-axis sputtering, but any deposition process may be used, including other forms of physical vapor deposition, chemical vapor deposition, metalorganic chemical vapor deposition, and even liquid phase epitaxy if that technique should evolve to the point of depositing high quality films.

In general, the highest quality YBCO films are made by an in situ deposition process, in other words, a process that does not require a high temperature post-deposition anneal to form the superconducting crystal structure. However, other workers in the art have reported producing high quality YBCO films by a so-called "barium fluoride" technique, in which the film is formed first in an amorphous structure which includes fluorine, then annealed at high temperature in an oxygen environment to drive out the fluorine, drive in the oxygen, and form the desired crystalline structure. The films of this invention may be made by the barium fluoride technique, in which case the appropriate annealing steps must be included.

If first substrate 12 is sapphire or silicon, the structure may also include a thin dielectric buffer layer deposited between layers 10 and 12. YBCO chemically reacts with sapphire and silicon, thereby degrading its superconducting properties. This degradation can be avoided by depositing one or more intervening buffer layers which do not react with either YBCO or the substrate material. Suitable buffer layer materials include strontium titanate, calcium titanate, magnesium oxide, and yttria-stabilized zirconia. Intervening buffer layers can also improve the epitaxy of the YBCO. An embodiment incorporating an intervening thin buffer layer 11 will be discussed later with respect to Figure 7.

Still with reference to Figure 2, substrate 12 has a thickness ST of perhaps 20 mils (508 microns) at this stage, which makes it reasonably stable and workable. This thickness makes the substrate 12 structurally stable and allows sufficient lateral heat conduction to thermally equalize its upper growth surface at a uniform constant temperature of approximately 750 degrees Celsius during the growth of superconducting layer 10. In the preferred embodiment, substrate 12 is held to the heater with a silver paste, clamped to a metallic foil, brazed with a silver alloy, or radiatively heated to ensure completely uniform temperatures over the growth surface.

Figure 3 shows the next stage of the process, in which a protective layer (or layers) 16 has been deposited over the superconductor layer 10. Protective layer 16 is used because some of the HTS crystalline phases, particularly with the YBCO compound, are unstable at the temperatures and pressures used in the deposition process. The materials tend to lose oxygen, which degrades their superconducting properties. For example, if low oxygen pressures are encountered at high temperatures, the orthorhombic YBCO phase will lose oxygen and may transform to an insulating phase with tetragonal symmetry or even decompose into species such as Y_2BCuO_5, $BaCuO_2$, and/or Cu_2O. In addition, YBCO is highly reactive with many substances and may degrade during subsequent processing steps without protection. Protective layer 16 controls oxygen diffusion and prevents chemical interaction or diffusion between superconductor layer 10 and subsequent bonding layers. Layer 16 may comprise silver, gold, or an oxide such as SiO_2 or Al_2O_3. Gold is preferred, since it is the most non-reactive element available and best controls chemical diffusion and oxygen loss. Alternatively, layer 16 may include a source of oxygen in the form of another YBCO layer or a layer of a different oxide material such as silver oxide, which decomposes at elevated temperatures to release oxygen.

In microwave technology developed for low Tc superconducting materials such as niobium, oxygen-reactive species such as chromium and indium alloys can be used in direct contact with, or in close proximity to, the superconducting films. Using these same methods with high Tc superconductors would cause loss of oxygen from the HTS film during the fabrication process and therefore degrade the superconducting properties. But materials such as silver, gold, and silicon dioxide cause minimal degradation and actually form protective barriers on the HTS films. Surface resistance of YBCO has been found to be not significantly affected by these materials.

In Figure 4, the structure shown in Figure 3 has been inverted and bonded to a carrier substrate 20 with suitable bonding layers 18. Bonding layers 18 may comprise elemental metals or metal alloys that are diffusion bonded or heat melted in place. These layers 18 may consist of thin metal foils or thin metal films deposited directly on layers 16 or 20 by chemical or physical deposition methods. Alternatively, organic adhesives may be used. If protective layer 16 is made from silver or gold, it could possibly also serve as the bonding layer 18. The bonding performed by the bonding layer is a mechanical bond; it can, but is not required to,

form a chemical bond as well. Carrier substrate 20 stabilizes the structure mechanically. Carrier substrate 20 is preferably made of the same material as the first substrate 12, or at least a substance having similar thermomechanical characteristics so as to eliminate mechanical stress during extreme temperature changes. Superconducting layer 10 is now sandwiched between the first substrate 12 and carrier substrate 20 which makes it possible to polish first substrate 12 to reduce its thickness to the desired value without danger of contaminating or physically damaging superconductor layer 10. In addition, substrate 12 is physically supported by carrier substrate 20 against physical fracture.

In Figure 5, the first substrate 12 has been polished to form a thin dielectric layer 12. The layer 12 may be machined or chemically etched to a thickness in the range of 1 to 250 microns, as desired, to form a dielectric layer for electronic circuits.

Finally, in Figure 6, a second superconductor layer 14 is deposited on dielectric layer 12. The second superconducting layer 14 may then be patterned by standard techniques to form the desired device. component, or circuit as discussed with respect to Figure 1. Heating is once again accomplished by brazing and/or clamping carrier substrate 20 to a heater or radiatively heating to facilitate high quality epitaxial growth of the second superconductor layer 14. Since the composite SDS structure is thicker than a single substrate, it may be necessary to supply more energy to the substrate heater in order to provide the optimal temperature at the growing surface.

Additional circuits may be added to the bottom of carrier substrate 20 in Figure 6, if desired, by depositing and patterning another layer of superconducting material thereon.

As mentioned earlier, it may be desirable to include a thin dielectric buffer layer 11 deposited between layers 10 and 12, as shown in Figure 7, to avoid having the superconducting layer chemically react with the substrate, thereby degrading its superconducting properties. This degradation can be avoided by depositing one or more intervening buffer layers 11 which do not chemically react with either the superconductor or the substrate material. Suitable buffer layer materials include strontium titanate, calcium titanate, magnesium oxide, and yttria-stabilized zirconia. Intervening buffer layers can also improve in-plane epitaxy of the superconductor. The structure of claim 7 is inverted and bonded to a carrier substrate 20 with bonding layers 18, in a manner similar to that of Figure 4. The substrate layer 12 is thinned into a suitable dielectric layer and a second intervening buffer layer 21 is deposited on layer 12 followed by a second superconductor layer 14 to form the SDS structure shown in Figure 8. Figure 8 is essentially the same structure as Figure 6, except including buffer layers 11 and 21.

The efficacy of this technique has been established by fabricating a microwave parallel-plate resonator using YBCO as the superconductor and gold for both the bonding layer 18 and the protective layer 16. Bonding was performed at a temperature of 800 degrees C. at an elevated uniaxial pressure. The resonator had a Q of approximately 6040 at a frequency of 6.41 GHz. In addition, gold and silver diffusion bonds have been used successfully to make double sided YBCO structures.

This invention is also appropriate for bismuthate superconductors such as $Ba_{1-x}K_xBiO_3$ or $Ba_{1-x}Rb_xBiO_3$. Bismuthates have lower superconducting transition temperatures but offer the advantages of a cubic structure and the opportunity to make hysteretic Josephson junctions, which might make it possible to integrate digital signal processing circuits based on familiar varieties of superconducting logic. Although the bismuthates are not susceptible to oxygen loss, they present similar problems with respect to forming two superconductor layers on opposite sides of a very thin dielectric.

This invention is appropriate for all known oxide superconductors and all known substrates on which HTS films are deposited including lanthanum aluminate, neodymium gallate, calcium neodymium aluminate, sapphire, silicon, lanthanum strontium gallate, and yttrium oxide. The substrate materials determine, to an extent, the quality of the superconducting films and the need for buffer layers but are otherwise not essential to the novelty of this invention.

The process described in this disclosure allows the creation of a never before obtainable structure that permits HTS microwave devices and circuits, as well as other impedance matched devices and circuits, to be fabricated with interlayer dielectrics over a wide range of thicknesses. In particular, the disclosed new process can be used to make denser circuits and higher frequency components than the prior art allows. Slight variations in the enumerated steps are, of course, possible. But the invention should be limited only in accordance with the appended claims and their equivalents.

Note that instead of thinning the original substrate to form the thin dielectric, it is also possible to thin the second-applied substrate instead. In the latter case the second superconductor would be formed over the thinned second substrate instead of the thinned first substrate.

Claims

1. A method of making superconducting electronic structures with superconducting layers on opposite sides of a thin dielectric layer, comprising the steps of:

forming a first layer of superconducting material on a first mechanically stable substrate;

forming a protective layer on said first layer of superconducting material;

attaching a second mechanically stable carrier substrate to said protective layer;

thinning said first substrate to form a dielectric layer; and

forming a second layer of superconducting material on the side of said dielectric layer opposite from said protective layer.

2. The method of claim 1 in which said second layer of superconducting material is patterned to form an electronic circuit structure.

3. The method of claim 1 in which said layers of superconducting material are formed by physical vapor deposition.

4. The method of claim 1 in which said layers of superconducting material are formed by chemical vapor deposition.

5. The method of claim 1 in which said superconducting materials are bismuthates.

6. The method of claim 1 in which said superconducting materials are cuprates.

7. The method of claim 6 in which said superconducting materials comprise YBCO.

8. The method of claim 7 in which said first substrate comprises lanthanum aluminate, magnesium oxide, or neodymium gallate.

9. The method of claim 8 in which said protective layer comprises a source of oxygen.

10. The method of claim 9 in which said source is YBCO.

11. The method of claim 9 in which said source is silver oxide.

12. The method of claim 8 in which said protective layer comprises gold, silver, or an alloy of gold and silver.

13. The method of claim 8 in which said protective layer is an oxide.

14. The method of claim 13 in which the oxide is SiO_2.

15. The method of claim 13 in which the oxide is Al_2O_3.

16. The method of claim 48 in which said bonding layer comprises an adhesive.

17. The method of claim 48 in which said bonding layer comprises gold, silver, or an alloy of gold and silver.

18. The method of claim 7 in which said first substrate comprises sapphire or silicon.

19. The method of claim 18 including the additional steps of depositing buffer materials between the YBCO layers and the first substrate.

20. The method of claim 19 in which said buffer materials are selected from the group consisting of strontium titanate, calcium titanate, magnesium oxide, and yttria-stabilized zirconia.

21. The method of claim 49 in which said bonding layer is an adhesive.

22. The method of claim 49 in which said bonding layer is a noble metal.

23. The method of claim 20, 21 or 22 in which said protective layer is a noble metal.

26. The method of claim 20, 21 or 22 in which said protective layer is silicon oxide or aluminum oxide.

29. A method of making superconducting microwave devices comprising the steps of:

forming a first layer of superconducting material on a first substrate;

forming a protective layer on said first layer of superconducting material;

attaching a second substrate to said protective layer;

thinning said first substrate to a thickness in the range of about 1 to 250 microns to form a dielectric layer suitable for the microwave region of the spectrum; and

forming a second layer of superconducting material on said dielectric layer to form signal conveying circuits.

30. A microwave circuit formed by the method of claim 2.

31. A microwave circuit formed by the method of claim 8.

32. A microwave circuit formed by the method of claim 20.

33. A microwave circuit formed by the method of claim 29.

34. A superconducting microwave circuit device comprising in combination:

a first layer of superconducting material;

a second layer of superconducting material patterned to form circuits; and

a dielectric layer between said first and second layers, said dielectric layer having a thickness in the range of about 1 to 250 microns.

35. The device of claim 34 in which said superconducting materials are cuprates.

36. The device of claim 34 in which said superconducting materials are bismuthates.

37. A superconducting electronic structure useful for supporting superconducting circuits comprising in combination:

a first substrate;

a layer of superconducting material epitaxially grown on the surface of said first substrate;

a protective layer on said layer of superconducting material on the side opposite from said first

substrate; and

a supporting substrate attached to said protective layer side of the layer of superconducting material.

38. The structure of claim 37 in which said supporting substrate is attached to said protective layer with a bonding layer, said bonding layer comprising a material selected form the group consisting of gold, silver, a gold and silver alloy, and an organic adhesive.

39. The structure of claim 37 in which the superconducting material is YBCO and the first substrate is lanthanum aluminate or magnesium oxide.

40. The structure of claim 37 in which the superconducting material is YBCO and the first substrate is sapphire or silicon and further including a buffer layer between said first substrate and said superconducting material.

41. The structure of claim 40 in which said buffer layer is a material selected from the group consisting of strontium titanate, calcium titanate, magnesium oxide, and yttria-stabilized zirconia.

42. The structure of claim 37 in which said first substrate is about 20 mils thick.

43. The structure of claim 42 in which said supporting substrate is attached to said protective layer with a bonding layer, said bonding layer comprising a material selected from the group consisting of gold, silver, a gold and silver alloy, and an organic adhesive.

44. The structure of claim 43 in which the superconducting material is YBCO and the first substrate is lanthanum aluminate or magnesium oxide.

45. The structure of claim 42 in which the superconducting material is YBCO and the first substrate is sapphire or silicon and further including a buffer layer between said first substrate and said superconducting material.

46. The structure of claim 45 in which said buffer layer is a material selected from the group consisting of strontium titanate, calcium titanate, magnesium oxide, and yttria-stabilized zirconia.

47. A method of thinning a substrate for superconducting electronic structures comprising the steps of:

forming a layer of superconducting material on a mechanically stable first substrate;

forming a protective layer on said layer of superconducting material;

attaching a mechanically stable carrier substrate to said protective layer; and

thinning said first substrate while said first substrate is supported by said carrier substrate.

48. The method of claim 1, wherein said step of attaching comprises the steps of:

forming a bonding layer on the side of said first protective layer opposite from said first layer of superconducting material; and

attaching said second mechanically stable carrier substrate to the side of said bonding layer opposite from said first protective layer.

49. The method of claim 20, wherein said step of attaching comprises the steps of:

forming a bonding layer on the side of said first protective layer opposite from said first layer of superconducting material; and

attaching said second mechanically stable carrier substrate to the side of said bonding layer opposite from said first protective layer.

50. A method of making superconducting electronic structures with superconducting layers on opposite sides of a thin dielectric layer, comprising the steps of:

forming a first layer of superconducting material on a first mechanically stable substrate;

attaching a second mechanically stable substrate to said first layer of superconducting material;

thinning a particular one of said first and second substrates to form a dielectric layer; and

forming a second layer of superconducting material on the side of said dielectric layer opposite from said first layer of superconducting material.

51. The method of claim 50, wherein said particular one of said first and second substrates is said first substrate, and wherein said step of attaching comprises the steps of:

forming a protective layer on said first layer of superconducting material; and

attaching said second mechanically stable carrier substrate to said protective layer.

FIG. 1

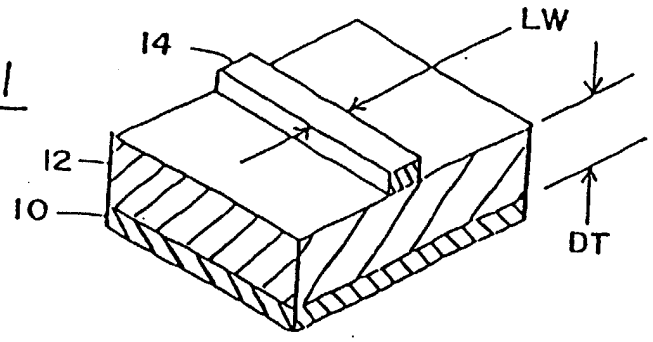


FIG. 2

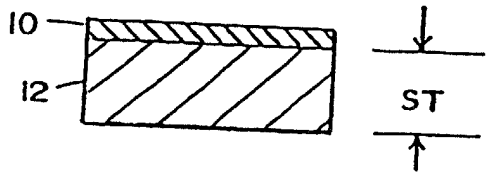


FIG. 3

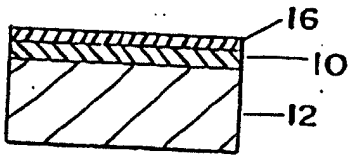


FIG. 4

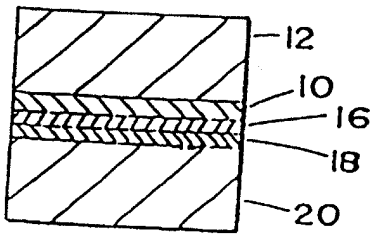


FIG. 5

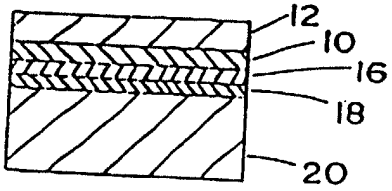


FIG. 6

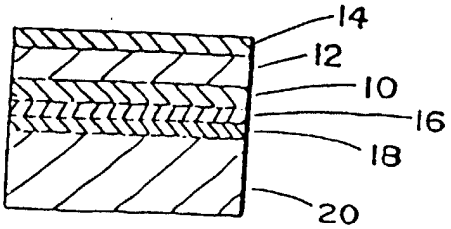


FIG. 7

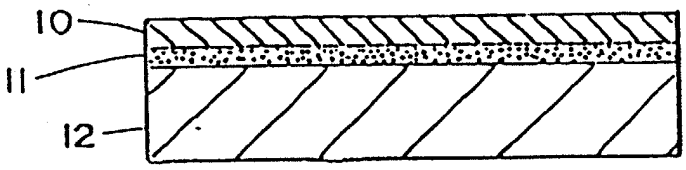
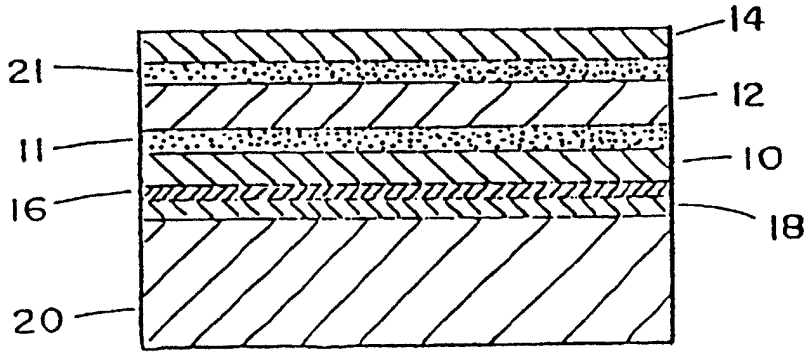


FIG. 8



European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 92 30 7681

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	DE-C-4 137 238 (DAIMLER-BENZ AG) * page 3, line 12 - line 67; figures 1A-1D *	1,3,4,6-8,29-31,33-35,37,50	H 01 L 39/24 H 01 L 39/14 H 01 P 3/08
A	EP-A-0 435 765 (SUMITOMO ELECTRIC INDUSTRIES, LTD.) * page 4, line 42 - line 54 * * page 8, line 21 - line 43; examples 1,3 *	1-3,5-8,18,19,29,30,31,33-37,40,44,45,	
A	EP-A-0 483 784 (SUMITOMO ELECTRIC INDUSTRIES, LTD.) * page 3, line 24 - line 36 * * page 4, line 45 - line 57; figure 2A *	2,5-8,19,20,40,41,45,46	
A	EP-A-0 345 441 (IBM CORP.) * page 5, column 16 - line 38; figure 2 *	1,29,34,37,48,50	TECHNICAL FIELDS SEARCHED (Int. Cl.5)
A	JAPANESE JOURNAL OF APPLIED PHYSICS, PART2, LETTERS vol. 30, no. 4B, 15 April 1991, TOKYO JP pages L700 - L702 A. TANAKA ET AL * page L700 *	2,5-8,34-36,39,44	H 01 L H 01 P
A	US-A-5 075 655 (J. M. POND ET AL) * abstract; figures *	1	
E	EP-A-0 508 893 (SUMITOMO ELECTRIC INDUSTRIES, LTD.) * page 3, line 1 - page 4, line 13; figures 1,2 *	1,29,34,37	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	26-04-1993	ROUSSEL A T

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
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E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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EP92307681

CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

☐ All claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for all claims.

☐ Only part of the claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid, namely claims:

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

LACK OF UNITY OF INVENTION

☒ The Search Division considers that the present European patent application does not comply with the requirement of unity of invention and relates to several inventions or groups of inventions, namely:

1. Claims 1-23,26,29-46,48-51: Two layers structure.

2. Claim 47: Method of thinning a substrate independant of two layers structure.

☐ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid, namely claims:

☒ None of the further search fees has been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims, namely claims: 1-23,26,29-46,48-51